Contrast Enhancement Materials for Yield Improvement in Submicron I-line Lithography

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ABSTRACT

Contrast Enhancement Lithography has been in existence for almost two decades, yet its practical advantages are relatively unknown among the general lithography community. This paper attempts to redress this situation by discussing the implementation of a Contrast Enhancement Material into manufacturing. Contrast Enhancement Materials (CEMs) are photobleachable solutions applied as a thin top coat to the photoresist after softbake. The CEM is initially opaque at the actinic wavelength but becomes essentially transparent upon exposure. Optimising the relative bleaching parameters of the photoresist and the Contrast Enhancement Material makes it possible to prevent exposure in nominally unexposed resist regions, while bleaching the exposed resist areas. Thus, a temporary contact mask is formed on the photoresist during exposure, allowing high-intensity parts of the aerial image to pass through while eliminating low intensity regions. The resulting aerial image which exposes the photoresist has higher contrast than the original. This allows superior resist depth-of-focus, improves resist profile, increases exposure latitudes and reduces proximity effects among other benefits. Initially, this paper discusses the chemistry and physics of the CEM process. Next the authors look at the lithographic requirements for a final metal level on a sub-micron CMOS process. Analysis of the Depth-Of-Focus error budget indicated that the process would not be manufacturable without significantly increased DOF. The authors also present the results of the characterisation of the CEM, including simulation work, with regard to the effect on primary lithography outputs such as depth-of-focus, resist sidewall and exposure latitude.

Keywords: Lithography, contrast enhancement, CEL, CEM, process latitude, yield

INTRODUCTION

Analog Devices has a 0.5um multi-level metal process in production. The minimum feature size at the final metal level is 0.9um. A focus and exposure error budget analysis[1,2,3] is shown in Figure 1.

Focus Control	**Focus Error (total range in nm)**	**Totals**	
Autofocus precision	100 nm (6 sigma)		
Best focus calculation	100nm (6 sigma)		
Daily Focus setup accuracy	240 nm (6 sigma)		
Sum total focus errors		278 nm 6 sigma	
Levelling			
Leveling repeatability	200 nm (6 sigma)		
Wafer non-flatness (SFQD)	300 nm (range)		
Stage unflatness	200 nm (range)		
Leveling Accuracy	150nm (6 sigma)		
Sum total random leveling errors		438 nm 6 sigma	
Field Deviations			
Reticle unflatness	40 nm (Range)		
Reticle sag	150nm (Range)		
Field Curvature and astigmatism	300 nm (Range)		
Sum total field errors		337 nm 6 sigma	
Topography			
Topography	2100nm (range)	2100 nm (range)	
Total Built-In Focus Error			2718 nm

Exposure Dose Contributions	Error	Total
Stepper Illumination uniformity (6 sigma) Dose reproducibility (6 sigma)	 1.5% 4%	 4.2% (6 sigma)
Substrate Reflectivity (6 sigma)	3%	3% (6 sigma)
Process Coat uniformity & reproducibility Bake uniformity & reproducibility Develop uniformity & reproducibility (6 sigma)	 5%	 5% (6 sigma)
Bulk and swing effect	5%	5% (range)
Total dose budget (RSS of random errors + systematic)		*12.2%*

Figure 1 – Focus and Exposure Error Budget Analysis for Metal Layer

As can be seen above, the DOF requirement is 2.72um with a concurrent exposure latitude requirement of 12.2%. However, at this exposure latitude the process has an available DOF of 2.3um, as will be demonstrated later. Since the available DOF is less than the Built-In-Focus-Error (BIFE) at this layer, the process has potentially poor manufacturability. The process of record without CEM utilizes a test wafer (send ahead wafer) to ensure the manufactured product retains high levels of quality. This procedure required a single wafer from each lot to be printed, CD measured, etched, CD measured again and finally inspected on a dark field defect inspection tool.

Although the test wafer procedure significantly reduced the scrap rate at this process stage, inevitable inefficiencies in the manufacturing process led to this test wafer adding significant cycle time delays. Also, even with the test wafer, the rework and scrap rates were still higher than normal.

Therefore, a more manufacturable process was required (where manufacturability is defined as the degree to which the process meets its focus and exposure error budget requirements).

A Contrast Enhancement Material was investigated to determine if it could provide the required process window. CMP was not a practical alternative due to the amount of process integration work required and the cost of the extra steps.

CONTRAST ENHANCEMENT MATERIALS

The Contrast Enhancement Material (CEM) process is a unique method/material designed to extend and enhance both the process latitude and resolution limits of optical lithography systems. CEM was developed by B.F. Griffing and P. West at GE to extend the limit of practical resolution in the field of microlithography. CEM-365iS[5] is an aqueous based contrast enhancement material (CEM). Non-aqueous CEMs require a barrier coat to prevent intermixing with the underlying resist layer.

As described by the manufacturer, CEM consists of a photobleachable material, which is initially opaque to the exposure wavelength(s) but becomes nearly transparent upon exposure. Figure 2 shows the spectral characteristics of CEM 365iS. The initial transmission at 365nm light is 11% +/- 1.5% with a final transmission of greater than 92%.

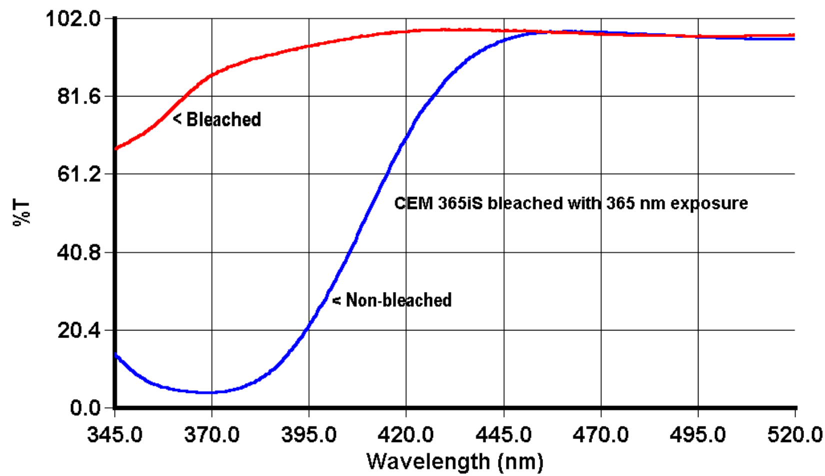


Figure 2 – CEM-365iS Spectral Characteristics

The thickness used is typically 0.4um. Figure 3 demonstrates the CEM principle. The CEM is spin coated over the positive resist. When an aerial image of a mask is incident upon the CEM layer, the regions of highest intensity (corresponding to the clear areas of the mask) are bleached at a faster rate than the lower intensity regions (the dark areas on the mask). By adjusting the bleaching dynamics such that the absorption of the CEM layer is sufficiently high and the photospeeds of the CEM and the resist layers are properly matched, it is possible to completely expose the underlying photoresist in the light areas before the CEM is bleached through in the dark areas. Thus, during the exposure an in-situ contact mask is formed in the CEM layer. The net effect is a higher contrast level of the aerial image used to expose the photoresist. The CEM process typically requires an exposure increase of 10-30%.

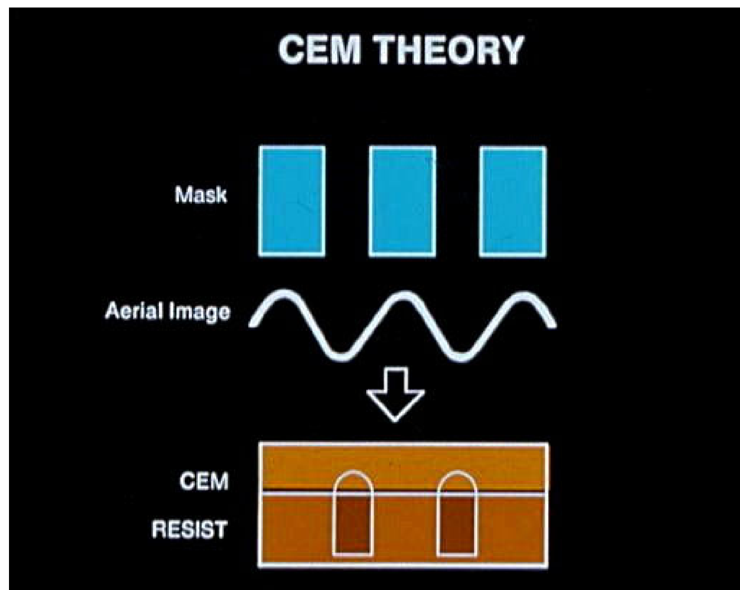


Figure 3 – CEM Principles

EXPERIMENTAL RESULTS

The following series of experiments were carried out using TEL Mk5z and ACT-8 tracks and Nikon i11 and i12 steppers. Numerical aperture settings were 0.5 (for investigation of metal substrates) and 0.6 (for use at 0.35um geometries on the poly gate level). CD metrology was performed using a Hitachi S9220 CDSEM, a Hitachi 4520 analytical SEM and defect inspection was performed using KLA AIT (dark-field) and KLA 2132 (bright-field) defect inspection tools.

The photoresists used were Shipley SPR955CM for metal layers and Shipley SPR660 for the poly gate layer.

The process conditions used with and without CEM are summarised in the following table.

Without CEM	
Step	**Conditions**
Prime	HMDS
Cool	
Coat	1.85um SPR955
Softbake	90 C/90 Sec
Cool	
Expose	0.5NA
Post-Exposure Bake	110 C/70 Sec
Cool	
Develop	55sec single puddle
Hardbake	

With CEM	
Step	**Conditions**
Prime	HMDS
Cool	
Coat	1.85um SPR955
Softbake	90 C/90 Sec
Cool	
CEM Coat	0.4um CEM-365iS
Expose	0.5NA
CEM Rinse	15 sec H20 rinse/spin
Post-Exposure Bake	110 C/70 Sec
Cool	
Develop	55sec single puddle
Hardbake	

Figure 4 – Metal Process With and Without CEM

RESULTS

1. Simulation
PROLITH/2[4] was used to simulate the performance of the CEM and was used to indicate whether the DOF increase would be significant enough to make the layer manufacturable once CEM was implemented.

Since resist sidewall angle through focus is the key metric for the metal layer, a process with CEM-365iS was compared to a process without CEM. It can be seen that the CEM gives substantial benefits in sidewall angle, particularly in the negative focus direction. Taking a required sidewall angle of 75 degrees, the CEM shows the potential of giving over 0.5um DOF increase.

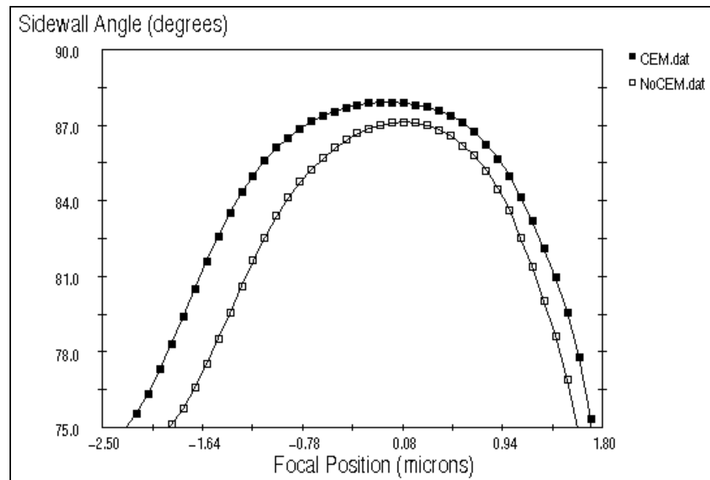


Figure 5 – PROLITH/2 Simulation of Metal Process

2. Final Metal Layer Wafer Results

For the final metal layer, a focus-exposure matrix was performed with and without CEM. Figure 6 shows the E-D window (plotted using ProDATA[4]) for the standard, no CEM, process. The bold line indicates the overlapping process window between dense (dotted line) and isolated (thin line) features. Figure 7 shows the equivalent process window for the CEM process. The sharp cutoff in the E-D window is evident in the negative focus region both with and without CEM and is due to unacceptable sidewall angle. However, the ability of the CEM to improve sidewall angle through focus allows the CEM process to have more focus latitude in the negative focus region. (Note the different horizontal scales in Figures 6 and 7.)

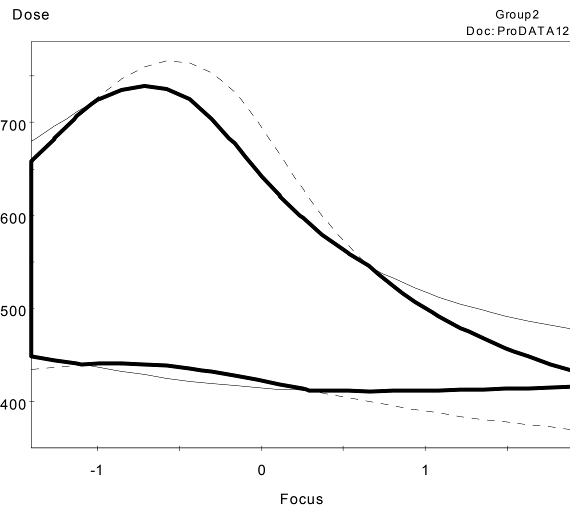


Figure 6 – No CEM E-D Window

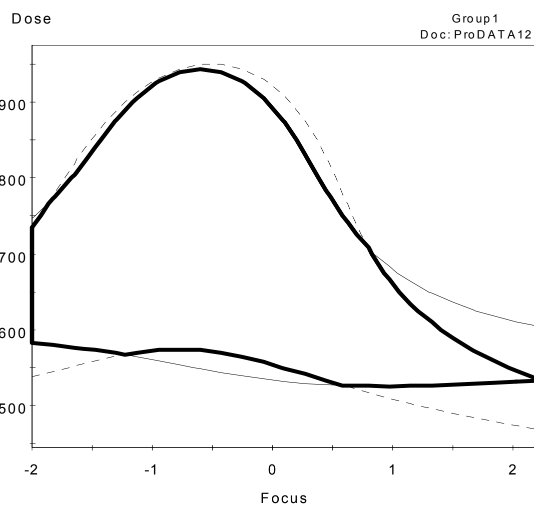


Figure 7 – CEM E-D Window

Figure 8 shows the DOF versus Exposure Latitude graph (derived by fitting various size rectangles in the overlapping process window and then plotting their width versus height). At the required exposure latitude of 12.2%, the CEM process has a DOF of approximately 3.0um. The standard process has a DOF of 2.3um at this exposure latitude. Therefore, the use of CEM increases the DOF by 30%, and allows the layer to meet the manufacturability requirement.

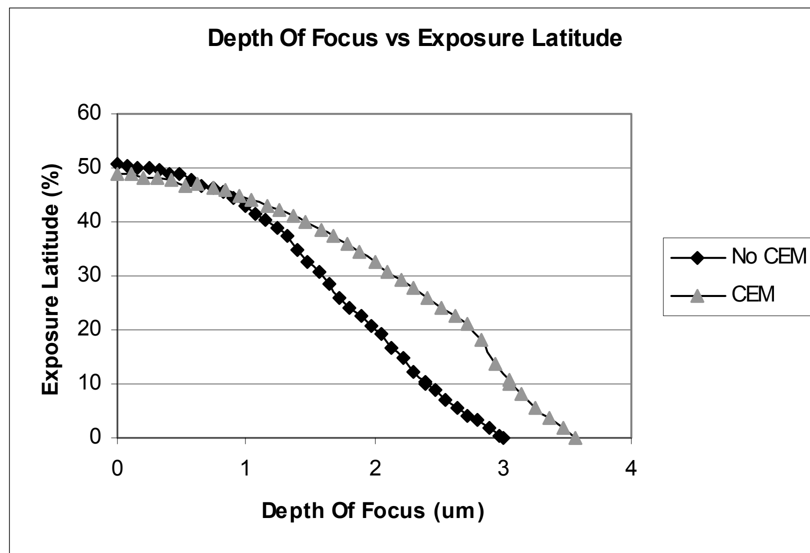


Figure 8 – DOF vs Exposure Latitude Curve

This superior resist performance translated into superior performance after etch as can be seen in Figure 9.

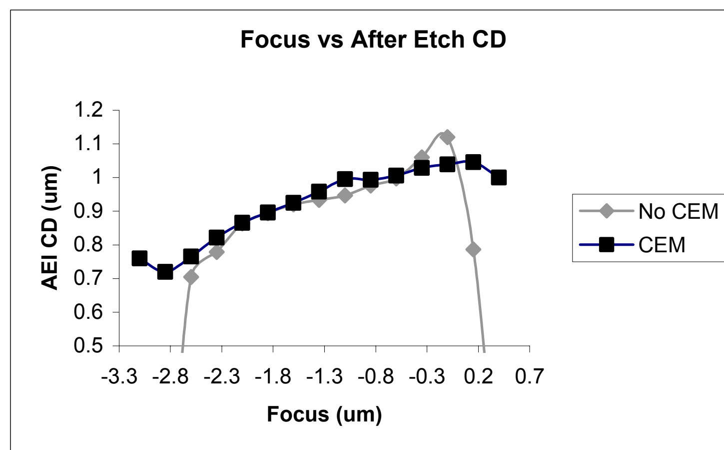


Figure 9 – After Etch CD Results

3. 0.35um Poly Gate Layer

A similar analysis was carried out on a 0.35um poly gate process. Figure 10 shows the overlapping E-D window for the standard process and Figure 11 shows the CEM E-D Window. The volume of the overlapping window is increased when using CEM primarily by the reduction in the proximity effect (i.e., iso-dense bias) and an increase in the dense line process window. The use of CEM is, therefore, beneficial across a range of process layers.

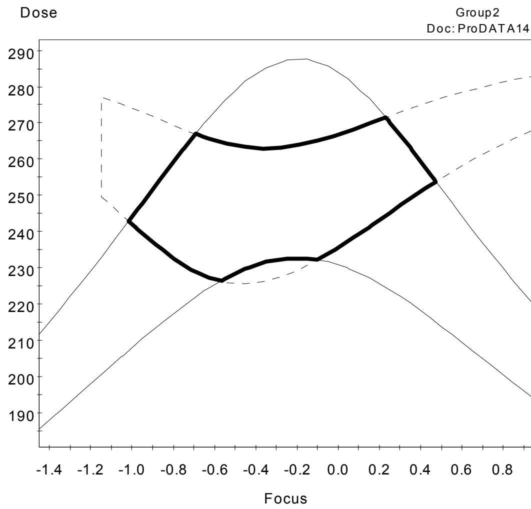


Figure 10 – E-D Window for No CEM

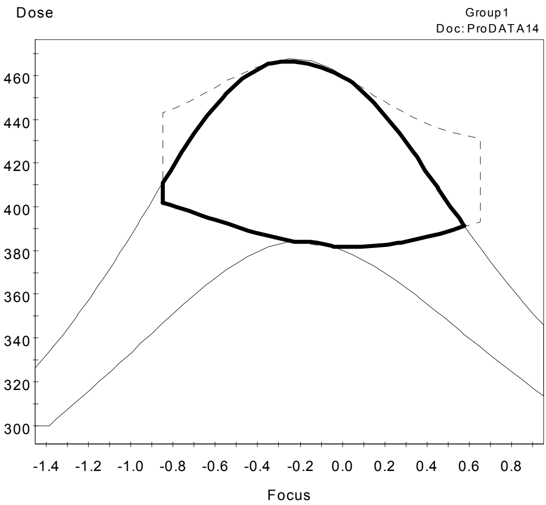


Figure 11 – E-D Window for CEM Process

4. Cross-Sectional Analysis on Metal for 0.9um Line/Space

The ability of CEM to deliver superior resist sidewall angle and reduced resist loss through focus is shown in the following cross-sectional analysis. The CD of the resulting etched metal line is more sensitive to these parameters than to base resist CD, due to the aggressive metal etch. Figure 12 shows the through-focus behaviour of 0.9um lines and spaces in 1.85um of resist. The reduced resist loss at negative focus when using CEM is evident.

Without CEM	With CEM	Focus	Without CEM	With CEM
		-2.8		
		-2.5		
		-2.2		
		-1.9		
		-1.6		
		-1.3		
		-1.0		

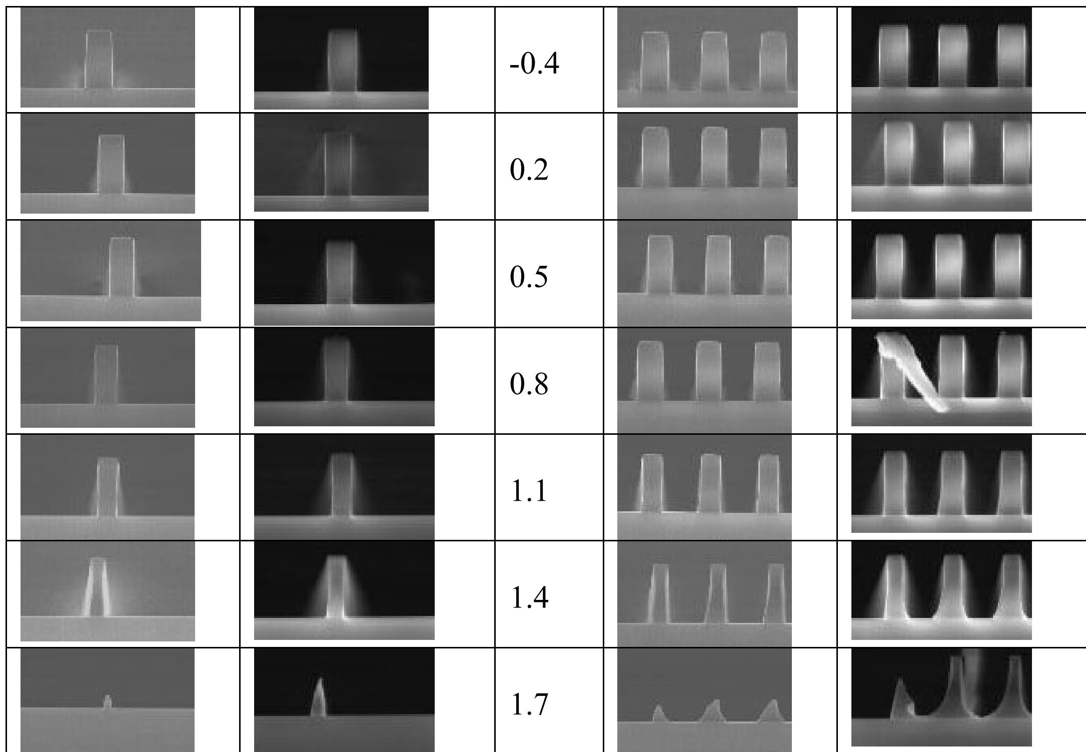


Figure 12 – Resist Cross-Section Through Focus

DEFECT WORK

The defect performance of the CEM process was compared to the standard process. Two different CEM processes are compared in Figure 13: one where the CEM was rinsed off before post-exposure bake, and one where the CEM was rinsed off after PEB and just before develop.

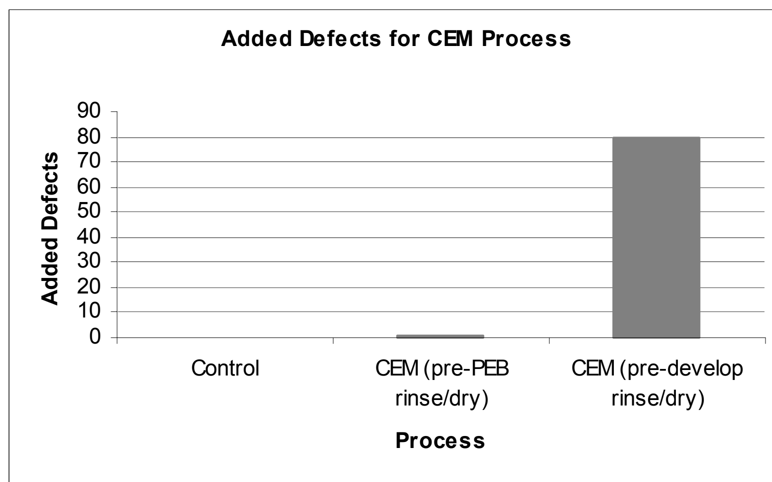
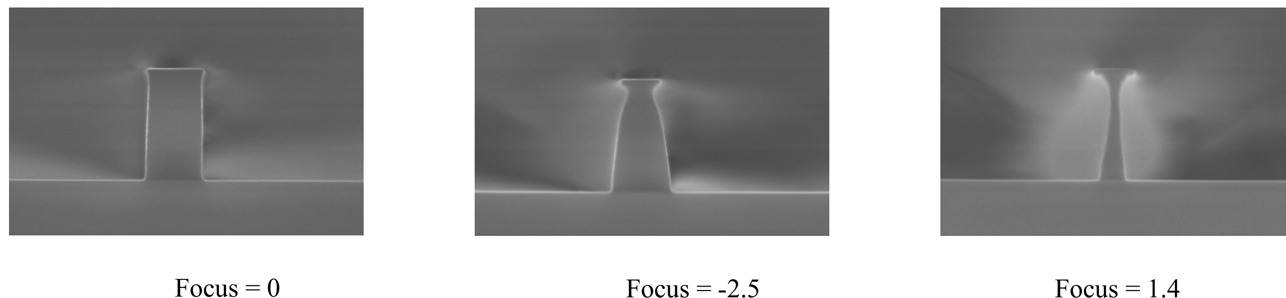


Figure 13 – Defects Added For Different CEM Processes

It can be seen that very high defect levels were seen in the latter process. These are attributed to the difficulty of rinsing (and spin drying) the CEM from the hydrophobic resist before develop. The added defects could be reduced to almost zero by rinsing the CEM from the wafer but without performing a spin dry. However, this would involve leaving a puddle of DI

water on the wafer before dispensing develop. This DI puddle tends to pull back from the wafer edges due to the low surface energy of the resist. This is expected to have a negative impact on cross-wafer CD control. It is believed that further work on optimizing the spin dry step would have led to a cleaner process. In any case, with the resist in question (and the given process conditions) a 't-topping' effect led to the choice of the pre-PEB rinse process. This effect is shown in Figure 14.



Focus = 0 Focus = -2.5 Focus = 1.4

Figure 14 – T-Topping Seen When CEM Is Not Rinsed Off Before PEB

This effect is attributed to the high temperature post-exposure bake causing a surface inhibition layer at the top of the photoresist when CEM is present. This effect is dependant on the resist properties and bake conditions. Whether this effect is indeed problematic at the metal level is perhaps arguable (i.e., since it only happens in out-of-focus conditions, perhaps it provides a level of protection to the underlying resist) , but it is likely to be undesirable at the poly gate layer due to its unpredictable effect on CD control. Rinsing the CEM off before PEB will eliminate this effect, should it occur.

YIELD

The success criteria for the CEM was for it to demonstrate that the process could be made manufacturable (i.e., sufficient DOF) without the necessity for a send-ahead wafer (the use of which essentially reduced the focus error budget). It was not necessary to demonstrate superior yield than the send-ahead wafer process. However, initial yield results across different parts indicated that a yield improvement of at least 2 percent occurred, although this was not statistically significant (p-value = 0.12). Figure 15 shows these initial yield results. The CEM process has higher mean, median and fewer low outliers.

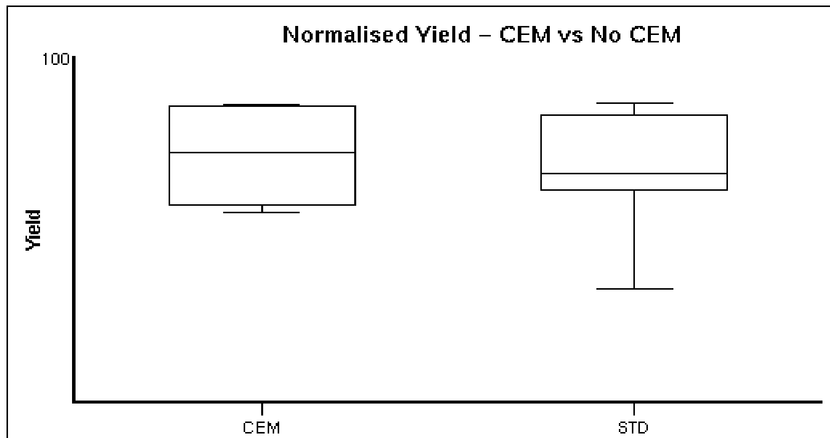


Figure 15 – Initial Yield Results

CONCLUSION

By implementing CEM 365iS with the existing resist process, we were able to improve the DOF by about 0.7um with sufficient exposure latitude. Due to the severe topography at the final metal level the DOF requirement is 2.7um but without

CEM, the DOF is 2.3um. With CEM, the process exceeds the DOF requirement. We have shown CEM to be easily implemented into the existing process with low defect levels and to show benefit at the 0.35um poly gate layer also. Contrast Enhancement Lithography proved capable of making the process manufacturable, thereby generating yield and reliability improvements while being less disruptive and costly than the alternative - the use of chemical mechanical polishing (CMP).

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REFERENCES

1. A. Grassmann *et* al, “How focus budgets are spent: limitations of advanced i-line lithography”, SPIE Vol. 2726, pp 386, 1996
2. C.A. Mack, “Understanding Focus Effects in Submicron lithography, part 3: Methods for DOF improvement”, SPIE 1674, pp272, 1992
3. K. Ronse *et al*, “CD Control: the limiting factor for i-line and DUV lithography?”, OCG Interface, pp241, 1995
4. PROLITH/2 and ProDATA, FINLE Division of KLA-Tencor
5. CEM-365iS is a trademark of Shin-Etsu MicroSi Inc.