Integrating ultra-thin Si dies within a flexible label

By Jean-Charles Souriau [CEA-Leti]

Recent developments in the integration of ultra-thin silicon dies within a flexible film lead to a new paradigm. Indeed, thanks to the thinness and flexibility of devices, it is conceivable that functions can be added around any object without changing its aspect [1-5]. Currently, only electronic tracks between components are flexible in the major flexible electronic products on the market. This is due to the fact that the silicon components are already packaged or are too thick. In order to get fully-flexible devices, silicon dies have to be thinned to less than 100µm. Three formats can be processed to build flexible electronic systems: ribbon, panel or wafer. The first two formats are well-adapted for large devices, are low cost, and allow high throughput. Patterning resolution in these formats is only fair, however. Working with silicon wafers helps achieve high resolution of integration. Silicon wafers are well-suited for flexible fan-out packaging, which helps build a heterogeneous, flexible system that combines a panel substrate, including a printed device and interconnection network with a silicon electronic die integrated within a small flexible label.

New process development

One challenge is to offer a process compatible with bare dies. A new technology called ChipInFlex proposes the integration of ultra-thin silicon dies within a flexible label made on a wafer carrier in the manufacturing microelectronic line [6]. It was chosen for the electrical interconnection gold stud bumps because it enables the hybridization by thermocompression at low temperature (<150°C) and it is compatible with the polymer (Figure 1). Indeed, the use of solder bump, such as SnAgCu, was not conceivable. Moreover, stud bumps also can be made on bare dies. The choice of the flexible material in which to integrate silicon dies is critical. In the ChipInFlex study, we tested the commercialized photosensitive siloxane polymer SiNR, which is available in spin-on or dry film, and has low stress and a low-cure temperature. The manufacturing process experiment is detailed in Figure 2.

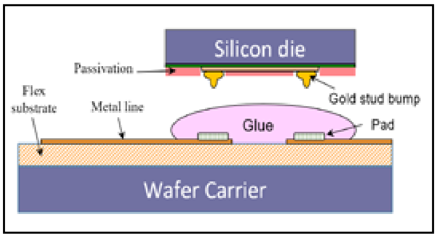

Figure 1: Flip chip Interconnection using gold stud bump.

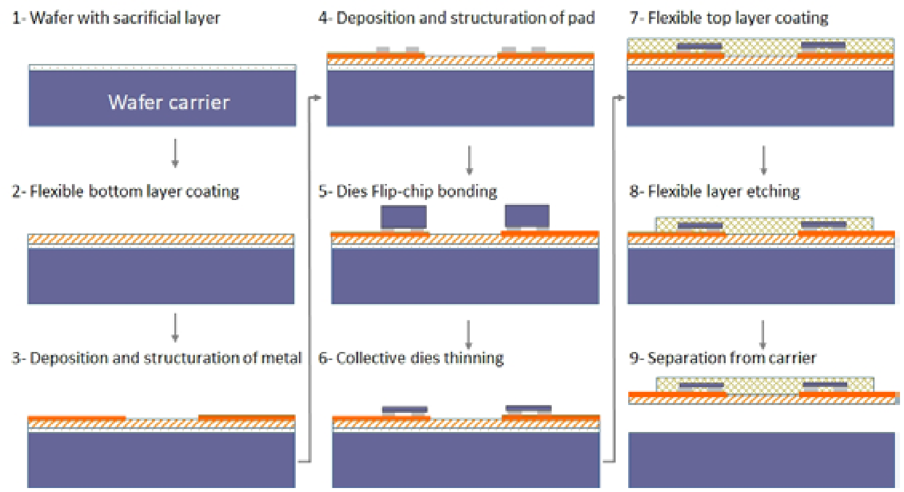

Figure 2: Wafer-level process flow of silicon dies' encapsulation.

The carrier is a 200mm silicon wafer, which was treated to get a temporary adhesion layer. A SINR film 30µm or 80µm thick was deposited by spin coating or laminating. The electrical network was made of WN_{50nm}/Au_{200nm} metallic. A 50µm-thick coating of silver glue was deposited on pads by serigraphy. Dies were aligned and attached on the wafer using a DATACON flip-chip tool. The equipment system enables dispensing dots of polymer glue and then aligns and mounts the components under a combination of heat and pressure. In this study, the Epo-Tek E505 glue was used because of its useful viscosity properties as a function of temperature. Stud bumps can easily go through the glue and contact gold pads on the substrate. The bonding was performed in two steps. All dies were attached with the flip-chip tool and then collectively bonded using an EVG thermocompression bonder. Collective thinning, including coarse and fine grinding, was performed

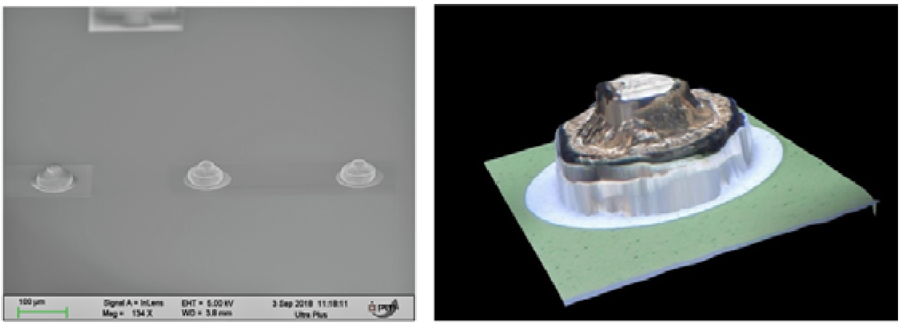

Figure 3: Gold stud bumps on a test vehicle.

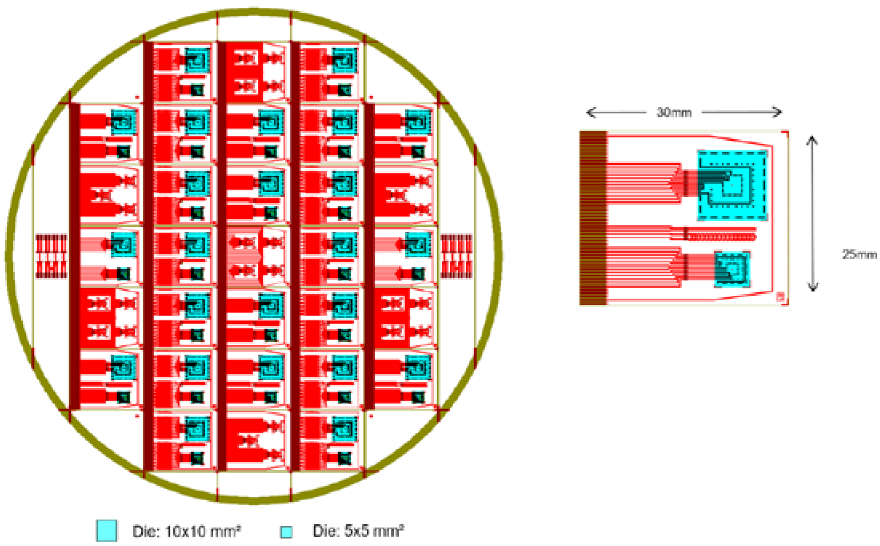

Figure 4: 200mm test vehicle wafer with 24 labels including large and small dies.

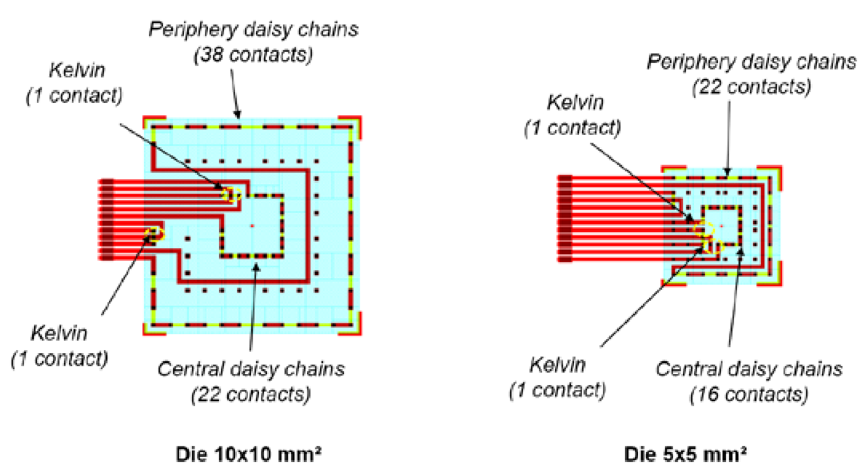

Figure 5: Layout overview of a four-point Kelvin pattern and daisy chains in silicon dies.

to reduce the die thickness to ~40µm. An additional 80µm-thick SINR layer was laminated under vacuum to encapsulate dies and the polymer was opened locally to reach metal lines and allow external connection. Finally, flexible labels were diced by laser and taken from the wafer carrier.

Results on electrical test vehicle

A silicon test vehicle was designed to mimic bare dies. Two sizes of chips were designed, 5x5mm² and 10x10mm², respectively. The test vehicle included 0.6µm-thick AlSi lines and passivation layers of SiO_2 (0.5µm thick), and SiN (0.6µm thick), respectively. Gold stud bumps were formed on pads using standard ball-bumping equipment. The stud bumps were approximately 70µm in diameter and 30µm in height (Figure 3).

The wafer included 24 30x25mm² labels and each one could receive one large and one small die (Figure 4). The test vehicle was designed to test the resistance of a single contact between the die and the flexible substrate thanks to a four-point Kelvin pattern. In addition, the continuity of daisy-chain structures, located at the periphery and at the center of the dies, could be measured (Figure 5). These patterns include from 16 to 38 contacts according to the size of dies and position.

Three wafers were fully populated and electrically characterized. Wafers 1 and 2 included a bottom polymer layer 80µm thick. Wafer 3 included a bottom polymer layer 30µm thick. For comparison, a fourth wafer without bottom polymer was populated only with small dies. Electrical tests were performed during the manufacturing process after the main steps, flip-chip bonding, backside thinning and final encapsulation (Figure 6). More than 90% of the Kelvin structure was functional. Global average values of Kelvin patterns are presented in Figure 7 and details for each location are shown in Table 1.

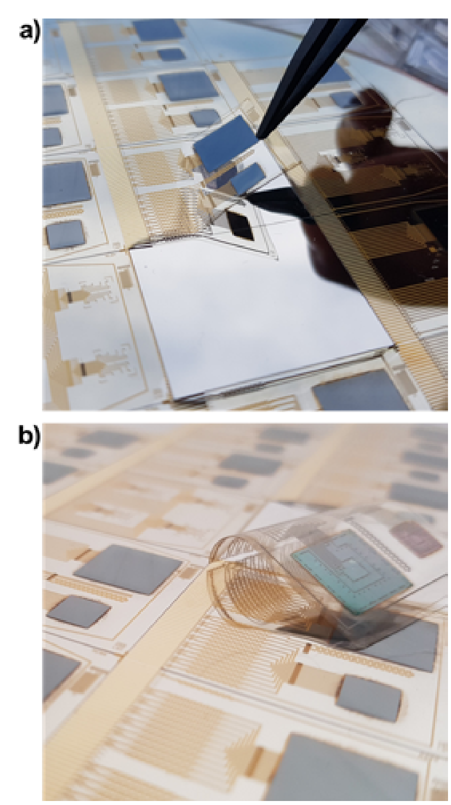

Figure 6: Label including silicon dies flip-chip bonded and thinned down to 40µm.

		Large dies		Small dies	
		Peripheral	Central	Peripheral	Central
Wafer 1	After bonding	11	14	14	11
	After thinning	11	15	15	11
	After coating	15	15	15	12
Wafer 2	After bonding	9	10	11	13
	After thinning	9	10	11	13
	After coating	11	11	12	13
Wafer 3	After bonding	6	9	7	9
	After thinning	6	9	7	9
	After coating	8	10	8	8

Table 1: Average resistance (in mOhm) of Kelvin patterns.

The final average resistance of a single contact was found to be from 12 to 14mOhms for wafers with an 80µm-thick bottom polymer, 9mOhms for the wafer with a 30µm-thick bottom polymer and 3mOhm for the wafer with no bottom polymer. The presence of a bottom polymer layer helped absorb the force on the stud bump during the thermocompression process and probably reduced the resistance value of the contact. No differences were observed between the center and the periphery of dies. Figure 8 shows the mapping of a central four-point Kelvin pattern measured on a small die on the periphery after final coating. The continuity of all the daisy chains was tested and the functionality rates are presented in Table 2 after each step.

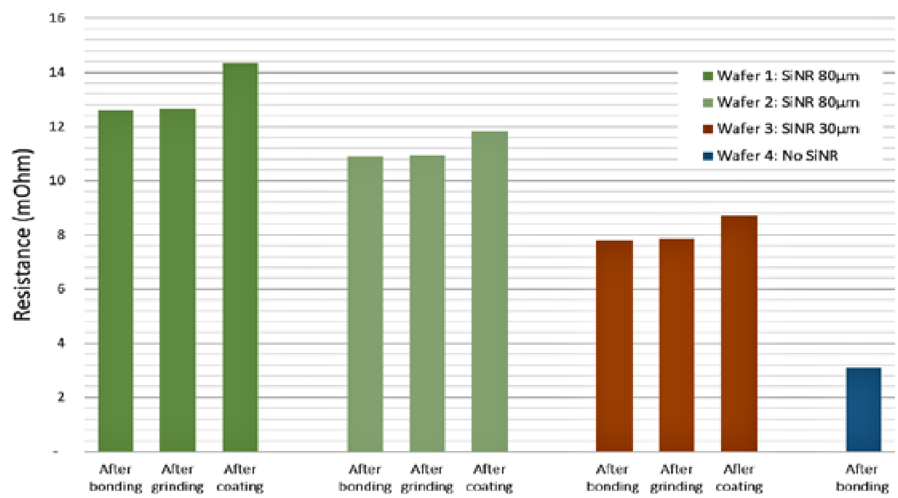

Figure 7: Global average resistance of Kelvin patterns measured after main steps of the process.

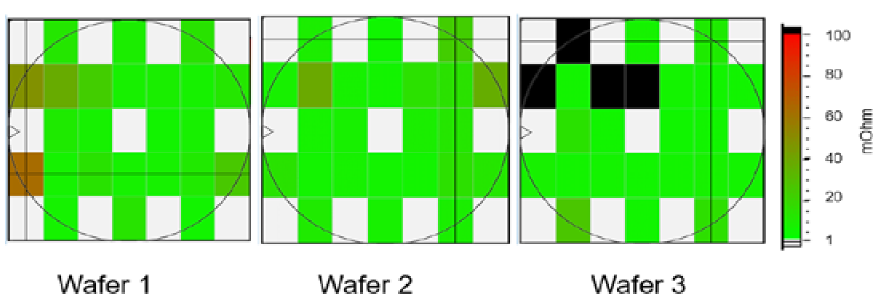

Figure 8: Resistance value mapping of a central four-point Kelvin pattern measured on small die in the periphery after final coating.

		Large dies		Small dies	
		Peripheral	Central	Peripheral	Central
Wafer 1	After bonding	87.5	100	87,5	100
	After thinning	87.5	100	87,5	100
	After coating	83.3	100	91.7	100
Wafer 2	After bonding	95.8	100	100	100
	After thinning	95.8	100	100	100
	After coating	91.7	100	100	100
Wafer 3	After bonding	100	100	100	100
	After thinning	100	100	100	100
	After coating	83	75	88	83

Table 2: Percentage of functional daisy chain after the main steps of the process.

	Line		Large die		Small die	
	Straight	Zigzag	Periph. daisy chains	Central daisy chains	Periph. daisy chains	Central daisy chains
Cal. value	56	51	67	39	59	43
Label n 1	62	50	65	40	53	41
Label n 2	58	45	68	39	53	39

Table 3: Resistance (in Ohm) measured of test patterns and compared with calculated values.

First, it can be noted that more than 87.5% of daisy chains were functional after bonding, which is a very good result for a new development. Moreover, the percentages of valid central daisy chains are excellent—100% for the three wafers. The most remarkable result from this study is that no failures occurred after thinning. It can be observed that yields are slightly reduced after coating, and few daisy chains failed. However, more data are needed to draw conclusions.

Two flexible labels were diced using a laser and removed from the wafer carrier. A printed circuit board (PCB) was designed and manufactured to facilitate electrical characterization. A ZIF connector was used to interconnect the label on the PCB (Figure 9). Six test patterns were measured. The first two patterns were just electrical tracks on the polymer without contact with the silicon die. The goal was to ensure that metal lines were not damaged by removing the label from the carrier. Peripheral and central daisy chain patterns of large and small dies were measured. Electrical results are summarized in Table 3 and compared with calculated values.

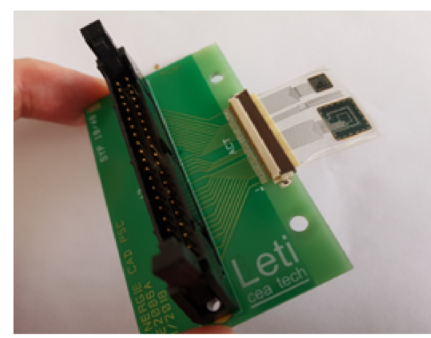

Figure 9: Printed circuit board to interconnect the label using a ZIF connector.

It has to be pointed out that all central daisy chains in the study were functional. Moreover, measurements closely agree with calculated values. More tests are ongoing on new labels to confirm these results.

Summary

With ChipInFlex, a new paradigm was introduced for integrating ultra-thin silicon bare dies within a flexible label made on the wafer carrier. ChipInFlex is a generic wafer-level process for manufacturing flexible labels and integrates silicon components. This process is the first to offer flip-chip silicon dies interconnected within a flexible film. The electrical interconnection is achieved with gold stud bumps made on bare dies. ChipInFlex is also the first packaging solution that can perform collective thinning on the wafer. The process has been successfully validated on an electrical test vehicle. A first step towards a complete electronic system in a flexible label has been made. CEA-Leti's packaging team is currently developing a demonstrator, with applications ranging from sensors to radio frequency identification (RFID) dies.

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Biography

Jean-Charles Souriau is project leader and scientific expert on wafer-level packaging at the U. Grenoble Alpes, CEA, Leti, Grenoble, France. He has a doctorate in Physics in 1993 from the Grenoble U. and has worked in the field of micro-interconnection and packaging for more than 20 years. He is the lead author of several publications and more than 10 patents. He is a senior member of the IEEE and president of the French chapter of the IEEE Electronics Packaging Society. Email: jean-charles.souriau@cea.fr